**AMENDMENTS TO THE SPECIFICATION**

Please replace the title as follows:

PLL/DLL DUAL LOOP DATA SYNCHRONIZATION ~~UTILLIZING~~ UTILIZING A GRANULAR FIFO FILL LEVEL INDICATOR

Please replace paragraph [0033] with the following amended paragraph.

[0033] Serializer system **500** included a PLL **502** and a DLL **504** in a dual loop configuration. In one particular embodiment, ~~DLL 504~~ PLL **502** is embedded within ~~PLL 502~~ DLL **504**; however, in other embodiments, the DLL and PLL may be separated. PLL **502** includes a phase frequency detector (PFD) **510**, a loop filter **512**, a VCO **514**, and a phase shifter **516**. DLL **504** also includes a phase detector **518** and a digital loop filter **520**. In addition, serializer system **500** includes a FIFO buffer **522** (first-in first-out) and a PISO (parallel-in serial-out) serializer **524**.

Please replace paragraph [0051] with the following amended paragraph.

[0051] **FIG. 8** illustrates an exemplary block diagram of a granular FIFO fill level indicator system **800**. FIFO fill level indicator system **800** is configured to facilitate the obtaining of a linear phase detector transfer function, which is highly desirable. Exemplary granular FIFO fill level indicator system **800** includes a write counter **802**, a plurality of FIFO registers **804**, a read counter **806**, and a comparison module **808**.

Comparison module **808** can comprise various devices and components for performing comparing functions, such as subtraction. In this particular embodiment, granular FIFO fill level indicator system **800** uses comparison module **808** to determine a difference between a state in write counter **802** and a state in read counter **806**. The difference is output from comparison module **808**, which performs the difference function, and represents the fill level of FIFO registers **804**. There may exist some difficulty in a direct implementation of FIFO fill level indicator system **800** because counters **802**, ~~**804**~~ **806** are generally asynchronous. In other words, the write clock and the read clock are not synchronized so the inputs received from counters **802** and **806** are generally not equally timed. Accordingly, the techniques to follow describe various embodiments for implementing a FIFO fill level indicator system **800** for data synchronization having asynchronous read and write clocks.